RANKFILTER IP PRODUCT BRIEF

Median, percentile and defect-pixel correction IP

Streaming 3×3 to 7×7 rank filters for FPGA and ASIC video, at 1, 2 or 4 pixels per clock. Fewer comparators per pixel, and each comparator network proved correct.

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RankFilter is a family of streaming two-dimensional rank filters for camera and video pipelines. Each output pixel is the median, or a chosen percentile, of its K×K neighbourhood. Defect-pixel correction (DPC) cores for raw Bayer and monochrome sensors replace only the pixels that stand out from their neighbours or that a factory defect map flags, which is how hot and dead pixels are usually corrected.

Each core is built from comparator networks, fixed sequences of compare-and-swap steps, and shares them between overlapping windows: a 5×5 median needs 52 comparators per output pixel, where column sharing (Adams 2021), the lowest published count we know of, needs 63. The comparator networks are proved correct in the Lean 4 proof assistant. Five cores ran a self-test on Altera Cyclone V silicon with zero CRC-32 mismatches against a reference model.

52
comparators per output pixel for a 5×5 median; column sharing (Adams 2021) needs 63

−75 %
LUTs against AMD's free Vitis Vision `medianBlur` at 5×5, same Vivado flow at 148.5 MHz (−83 % at 7×7)

4K60
at 4 pixels per clock with 4K line buffers, every 4 px/clk core: AMD Artix 7, Zynq and the slowest Cyclone V grade

0
CRC-32 mismatches in about 22 million self-test runs on Cyclone V silicon

Features

- Median of 3×3, 5×5 and 7×7 windows; 25th and 75th percentile of 5×5
- DPC for Bayer and monochrome sensors with a run-time threshold; the monochrome core also takes a static defect map
- SEU-tolerant monochrome DPC cores that recover from single-event upsets without a reset (simulation fault injection)
- 1, 2 or 4 pixels per clock
- AXI4-Stream video with full back-pressure, or a smaller video-timing version for streams that cannot stall
- Frame size set at run time; replicate or constant borders
- Pixel width set by a parameter; every core frame-tested at 8 to 16 bits
- Credit-based flow control, formally proved never to drop or overwrite data (the SEU-tolerant cores excepted while they flush after an upset)
- Plain Verilog-2005 with inferred block RAM; Vivado IP Integrator, Quartus Platform Designer and VHDL packages

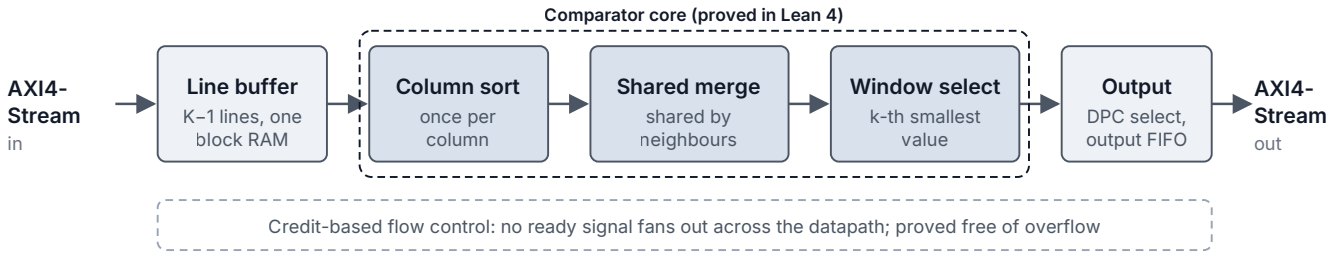
Applications

- Hot and dead pixel correction on colour, thermal and SWIR sensors
- Impulse (salt-and-pepper) noise removal
- Pre-processing for machine vision and industrial inspection
- Rank-order filtering in scientific, medical and broadcast imaging
- Space imaging payloads (SEU-tolerant cores)

Supported devices

Any FPGA or ASIC flow that accepts Verilog-2005. Measured on AMD Artix 7, Zynq 7000 and Zynq UltraScale+ (Vivado), Altera Cyclone V (Quartus), Lattice ECP5, and the SkyWater 130 nm and ASAP7 PDKs.

Block diagram



Border handling is inside the line buffer stage. The DPC select stage is present in the defect-pixel correction cores only.

Resources and Fmax, complete filter, 8-bit pixels

	AMD Artix 7 −1, Vivado			Altera Cyclone V C8, Quartus (Fmax: lowest of 3 seeds)			Lattice ECP5 −6, nextpnr (Fmax: lowest of 5 seeds)		
Core	LUT	FF	Fmax	ALM	M10K	Fmax	LUT4	DP16KD	Fmax
3×3 median	345	567	237	371	7	180	928	2	146
3×3 median, 4 px/clk	974	1,526	237	939	8	180	2,233	8	126
5×5 median	871	1,511	209	896	10	180	2,056	4	162
5×5 median, 4 px/clk	2,638	3,766	225	2,216	28	163	5,184	15	154
5×5 25th percentile	751	1,302	238	769	10	180	1,783	4	163
7×7 median	1,969	3,458	217	1,941	20	167	4,455	6	150
7×7 median, 4 px/clk	5,534	7,976	215	5,276	46	152	11,452	23	128
Bayer DPC	410	771	228	435	9	159	1,092	4	159
Bayer DPC, 4 px/clk	1,197	1,860	215	1,115	11	180	2,673	15	150
Mono DPC with defect map	384	633	214	430	7	180	959	2	160

Complete filter: AXI4-Stream wrapper, line buffers for 2,048-pixel lines, border logic and comparator core; 1 px/clk unless stated. Fmax in MHz, slowest speed grade of each family. Artix 7 xc7a35t-1: Vivado 2025.2, filter instance only, resources at 148.5 MHz. Cyclone V 5CEBA4F23C8: Quartus Prime Lite 19.1, lowest of 3 seeds (2 for the monochrome DPC), with a small measurement harness; 180 MHz is the M10K block RAM's limit. ECP5 LFE5U-85F: yosys and nextpnr, lowest of 5 seeds (3 for the monochrome DPC), with the harness.

1080p60 needs 148.5 MHz at 1 px/clk; on ECP5 −6 the 3×3 core meets it on 4 of 5 seeds. 4K60 at 4 px/clk needs 4,096-pixel lines and 148.5 MHz, or 124.4 MHz at the active pixel rate. With 4K lines each 4 px/clk core meets 148.5 MHz on the AMD parts and on all Cyclone V seeds, and ECP5 −6 meets the active rate for each 4 px/clk core except the 7×7.

Comparators per output pixel

Window, px/clk	RankFilter	Adams method	Single window	Odd-even
3×3, 1	13	13†	19	36
5×5, 1	52	63	85	300
5×5, 4	37	42.75†	85	300
7×7, 1	140	187	231	1,176
7×7, 2 / 4	92	117† / 93.25	231	1,176

Adams 2021 (ACM Transactions on Graphics) is a software method that computes tiles of outputs. 187 and 93.25 are published in the paper and 63 is derived from it; † marks our own count for the Adams method. Single window: the smallest known networks that sort one whole window, with no sharing. Odd-even: the transposition sort that Vitis `medianBlur` unrolls. Only the RankFilter column is proved.

Against other designs, same flow

Comparison	5×5	7×7
AMD Vitis Vision `medianBlur`, Artix 7 LUT	−75 %	−83 %
Same, at 4 px/clk	−64 %	Vitis does not fit
Baseline, Artix 7 LUT	−14 %	−26 %
Baseline, Cyclone V ALM	−18 %	−22 %
Baseline, ECP5 LUT4	−11 %	−21 %
Baseline, sky130 area	−16 %	−25 %

Same harness, flow, part and line length for both designs; AMD resources at a common 148.5 MHz constraint. Baseline: column sharing (each column sorted once, then a selection network), built with the same generator and wrapper. Vitis: Vitis_Libraries 2025.2, the better of two builds per metric; each build compared was simulated and gives the correct median. Its 7×7 at 4 px/clk does not fit the xc7a35t.

Verification

- Comparator networks proved in Lean 4 for any input.
- RTL simulated on all windows of 0s and 1s (all 2^{25} at 5×5; at 7×7 all columns and sorted-column combinations); a comparator network correct for all 0-1 inputs is correct for all inputs (the 0-1 principle).
- Flow control proved with SymbiYosys (SEU-tolerant cores: outside a flush).
- Photographs byte-identical to an independent reference model.
- Cyclone V silicon: about 22 million soak-test runs of two 320×240 frames under random back-pressure, zero CRC-32 mismatches.

Deliverables

- Verilog-2005 source for each licensed core: an FPGA set and an ASIC-tuned set
- Vivado IP Integrator packages, Quartus Platform Designer components and a VHDL component package
- Bit-exact Python reference model and golden test vectors
- Self-checking SystemVerilog testbench; board self-test with an expected CRC-32
- Lean 4 proof files
- Datasheets DS-RF-01 to 04, comparison brief CB-RF-01, integration notes; product guides PG-RF-01 to 04 on request

Evaluation and licensing
Source code, per project or per company; pricing and terms on request. Simulation evaluation package on request. Other window sizes, ranks, pixel widths and pixels per clock are generated to order.

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