RANKFILTER IP CORE DATASHEET

SEU-tolerant defect-pixel correction

Monochrome defect-pixel correction that recovers from single-event upsets without a reset

Datasheet DS-RF-04 · Revision 1.0 · 2026-10-14 · Bumble Bytes Ltd

Description

These are the monochrome defect-pixel correction (DPC) cores of datasheet DS-RF-03 with self-checks on their control logic. When a single-event upset (a particle flipping a flip-flop, in orbit or at altitude) corrupts the control state, the core clears it, raises `seu_err` and resumes with the next frame, with no reset; clean output returns within about two frame periods. In simulated fault injection none of 8,000 random flip-flop upsets needed a reset; the default core needed one in 4.7 %.

The checks compare the core's own control registers every clock. The relations they test are proved to hold whenever there is no upset, so a failed check means an upset. Pixel data and the line buffer are not checked: an upset there changes a few pixels of one frame, as in the default cores. On Artix 7 the checks cost 72 LUTs and no block RAM.

Function, parameters, ports and timing are those of the default cores, plus the `seu_err` output, so the cores drop in where the default cores are used. The upset figures come from simulation; the cores have not been tested in a particle beam.

Applications

- Space imaging payloads: thermal, SWIR and visible monochrome cameras, star trackers
- High-altitude imaging, and cameras near accelerators or other radiation sources, where a stalled video stream costs more than a lost frame

FUNCTION

- Defect map, threshold and 3×3 median, as the monochrome DPC cores
- AXI4-Stream core: 12 registered checks on credit counts, queue and FIFO pointers and the latched frame size
- Video-timing core: parity over the latched frame size
- Line and frame ends tested with ≥, so a corrupted counter cannot run on until it wraps

RECOVERY

- A failed check clears the control path; the core resumes with the next frame
- Clean output within about two frame periods, with no reset
- `seu_err`: a sticky flag for health monitoring

PERFORMANCE AND SIZE

- 1 pixel per clock; 1080p60 from the 148.5 MHz pixel clock on all measured FPGA families (AMD at 8 bits)
- Artix 7: +19 % LUTs (AXI4-Stream), +8 % (video timing); same block RAM
- Longest line 2,048 pixels by default; latency 1 line + 21 clocks

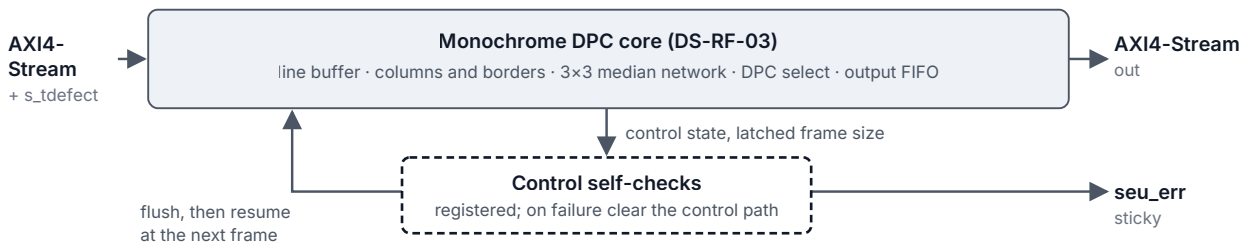
VERIFICATION

- No false alarms: formally proved (SymbiYosys) for frame sizes in range
- Simulated fault injection, 8,000 random flip-flop upsets per core

INTEGRATION

- Ports of the default cores plus `seu_err`; one clock, synchronous reset
- Vivado 2025.2 IP Integrator, Quartus Platform Designer and VHDL packages; ASIC set

Block diagram



The checks see control state and the latched frame size only. An upset in pixel data or the line buffer changes at most a few pixels of one frame, as in the default cores.

Implementation results

Device and resource	AXI4-Stream	AXI4-Stream _seu	Video timing	Video timing _seu
AMD Artix 7 xc7a35t-1, 8 bits · Vivado 2025.2				
LUTs	384	456	263	283
Flip-flops	633	673	536	539
Block RAM (RAMB36)	1	1	1	1
Fmax (MHz)	214	225	235	239
AMD Zynq UltraScale+ xczu3eg-1, 8 bits · Vivado 2025.2				
LUTs	390	456	267	289
Fmax (MHz)[1]	571	571	571	571
Altera Cyclone V 5CEBA4F23C8, 14 bits · Quartus Prime Lite 19.1				
ALMs	655	687	521	518
Block RAM (M10K)	10	9	6	6
Fmax (MHz), lowest of 2 seeds[2]	179	155	177	166
Lattice ECP5 LFE5U-85F −6, 14 bits · yosys and nextpnr				
LUT4s	1,385	1,497	910	1,035
Flip-flops	1,546	1,581	1,267	1,270
Block RAM (DP16KD)	4	4	4	4
Fmax (MHz), lowest of 3 seeds	151	150	156	165

Figures are for the complete core with the defect map and a 2,048-pixel line buffer, at the slowest speed grade. AMD: post-route, filter alone, resources at 148.5 MHz, Fmax from a separate sign-off run per design. Cyclone V and ECP5 include a small test harness. [1] Block RAM clock limit of the −1 part. [2] Cyclone V C8 limits M10K to 180 MHz.

Fault-injection results

One upset per run	AXI4-Stream	AXI4-Stream _seu	Video timing	Video timing _seu
Needs `rst`: random flip-flop	4.7 % (374 of 8,000)	0 of 8,000	0 of 8,000	0 of 8,000
Needs `rst`: each control bit ×10	27.3 % of 3,710	0 of 4,100	0 of 1,800	0 of 1,830
Frame periods to clean output (random flip-flop, longest)	11,425	1.9	7,698	2.1

Verilator, 14-bit pixels with the map, 2,048-pixel line buffer, 64×16-pixel test frames, random data and back-pressure; same seeds for each pair. 95 % interval for 4.7 %: 4.2 to 5.2 %. In 1.0 % (AXI4-Stream) and 2.4 % (video timing) of random upsets the default core's row counter runs on until it wraps, losing up to 2^{16} input lines and adding up to 2^{17} output lines: about 3 s for a 1,024-line sensor at 60 frames per second (estimate from the counter widths), shown here as 11,425 and 7,698 periods of the 16-line test frame. In all campaigns the `_seu` cores lost at most 2 frames.

Verification

SymbiYosys proves that, with frame sizes in range, `seu_err` never rises without an upset, and that the default cores' flow-control properties hold outside a flush. A flush drops the frames inside the core and may lower `m_tvalid` without a handshake, as a reset does (86 of 8,000 random upsets). Without upsets, 81 regression runs and 12 golden images match the default cores. Not covered: multiple-bit upsets, clock and reset nets, and configuration memory, which needs the vendor's scrubbing.

Core family

Module	Interface
`rankfilter_dpc3_p1_seu`	AXI4-Stream
`rankfilter_dpc3_p1_v_seu`	video timing

1 pixel per clock. The ASIC set has the same cores with `_asic_seu`; the default cores are in DS-RF-03.

Deliverables

- Verilog-2005 source, FPGA and ASIC sets
- The integration packages listed above
- Reference model, vectors, self-checking testbench
- Fault-injection results, Lean 4 proofs, a one-page SEU note

Licensing: source code, per project or per company; pricing and terms on request. Simulation evaluation package on request.

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