RANKFILTER IP CORE DATASHEET

Monochrome defect-pixel correction

Bad-pixel map and threshold correction for thermal, SWIR and scientific sensors

Datasheet DS-RF-03 · Revision 1.0 · 2026-10-14 · Bumble Bytes Ltd

Description

The RankFilter monochrome defect-pixel correction (DPC) cores replace bad pixels in thermal, SWIR and scientific video with the median of their 3×3 neighbourhood. They correct both the sensor's factory defect map, fed in as a per-pixel flag, and pixels that fail in service, found by a run-time threshold. Every other pixel passes through unchanged.

The flag arrives with each pixel on its own input, so the pixel keeps the sensor's width, typically 14 bits for thermal cameras. The core stores two lines and one flag bit per pixel in a single block RAM word, so the map needs no extra block RAM. At 14 bits the complete core uses 655 ALMs and 10 M10K on Cyclone V.

The median comes from the same comparator network as the other RankFilter 3×3 cores, a fixed sequence of compare-and-swap steps proved correct in the Lean 4 proof assistant. The flow control is formally proved with SymbiYosys. Each core is one Verilog-2005 file using only inferred block RAM, so it suits any FPGA or ASIC flow. SEU-tolerant variants for space and other radiation environments are described in datasheet DS-RF-04.

Applications

- Thermal (LWIR, MWIR), SWIR and InGaAs camera cores
- Scientific, X-ray and astronomy cameras; line-scan and spectral imagers
- Space imaging payloads, with the SEU-tolerant cores

FUNCTION

- Replace a pixel by its 3×3 median when its defect flag is set, or when |pixel − median| > `cfg_dpc_thr`
- Map only, threshold only, or both; correction off gives a plain 3×3 median
- Corrects isolated pixels, 2×2 clusters and single bad rows or columns

INTERFACES

- AXI4-Stream video with full back-pressure and a per-pixel defect flag, `s_tdefect`
- Video-timing variant for sources that cannot stall
- One clock; synchronous reset (`aresetn` in the Vivado package)

PERFORMANCE AND SIZE

- 1 pixel per clock; 1080p60 from the 148.5 MHz pixel clock on all measured FPGA families, at 8 and 14 bits (AMD at 8 bits)
- Longest line 2,048 pixels by default (parameter `AW`); latency 1 line + 21 clocks
- Pixel width set by a parameter; tested at 8 to 16 bits

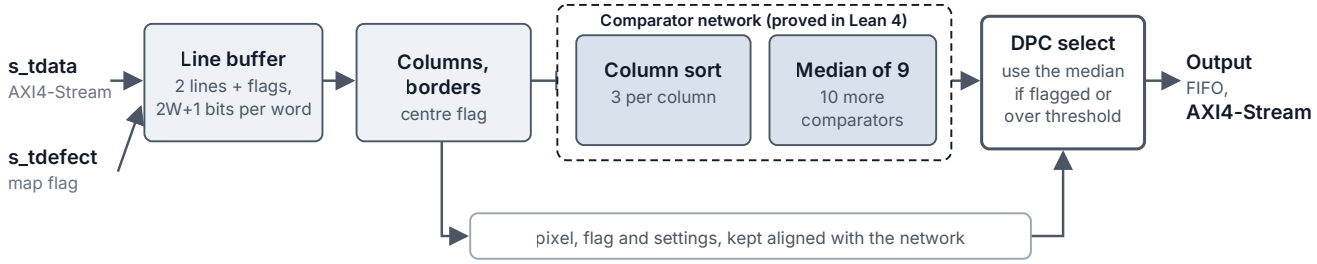
VERIFICATION

- Median network proved correct in Lean 4
- Flow control formally proved (SymbiYosys)
- Code coverage: 100 % of blocks, 98 % of branches

INTEGRATION

- One Verilog-2005 file per core, for any FPGA or ASIC flow
- Vivado 2025.2 IP Integrator (flag on TUSER[1]), Quartus Platform Designer and VHDL packages; ASIC set

Block diagram



Video-timing variant: no queue or output FIFO; s_tready is low only inside the blanking windows.

The DPC select stage takes two clocks: subtract, then compare and select. The 3×3 network uses 13 comparators per pixel.

Implementation results

Device and resource	AXI4-Stream, 8 bits	AXI4-Stream, 14 bits	Video timing, 8 bits	Video timing, 14 bits
AMD Artix 7 xc7a35t-1 · Vivado 2025.2				
LUTs	384	–	263	–
Flip-flops	633	–	536	–
Block RAM (RAMB36)	1	–	1	–
Fmax (MHz)	214	–	235	–
AMD Zynq UltraScale+ xczu3eg-1 · Vivado 2025.2				
LUTs	390	–	267	–
Fmax (MHz)[1]	571	–	571	–
Altera Cyclone V 5CEBA4F23C8 · Quartus Prime Lite 19.1				
ALMs	430	655	316	521
Block RAM (M10K)	7	10	4	6
Fmax (MHz), lowest of 2 seeds[2]	180	179	180	177
Lattice ECP5 LFE5U-85F –6 · yosys and nextpnr				
LUT4s	959	1,385	655	910
Flip-flops	1,026	1,546	831	1,267
Block RAM (DP16KD)	2	4	2	4
Fmax (MHz), lowest of 3 seeds	160	151	161	156

Figures are for the complete core with the defect map and a 2,048-pixel line buffer, at the slowest speed grade. –: the Vivado runs are at 8 bits only. AMD: post-route, filter alone, resources at 148.5 MHz, Fmax from a separate sign-off run per design. Cyclone V and ECP5 include a small test harness. [1] Block RAM clock limit of the –1 part. [2] Cyclone V C8 limits M10K to 180 MHz. Builds without the map and Zynq 7000: product guide PG-RF-03 (available on request).

Comparison

The line buffer needs about half the bits of a Bayer DPC core (2W + 1 per word against 4W): 2 against 4 DP16KD on ECP5 at 8 bits (4 against 7 at 14), 1 against 2 RAMB36 on Artix 7, and 7 against 9 M10K on Cyclone V (10 against 15 at 14 bits). Against a plain 3×3 median on Cyclone V, correction adds 59 ALMs (AXI4-Stream) and 39 (video timing); the map alone adds 1.1 to 3.6 % ALMs.

Verification

Lean 4 proves the 3×3 median network for any ordered pixel type; the correction stage is verified by simulation and coverage. SymbiYosys proves the flow control. Both cores match a bit-exact reference model with and without the map, with full-rate, stalled and random back-pressure, on frames from 1×1 to 1080p and at 8 to 16 bits; twelve golden images with a 945-pixel defect map are byte-identical to an independent model. In 73,577 malformed-input runs across all 24 RankFilter cores, no core hung, and each returned to correct output by itself. Code coverage: 100 % of blocks and expressions, 98 % of branches and 99 % of toggles; the rest was reviewed. These two cores have not yet run on silicon; the median and Bayer cores of the same family have.

Core family

Module	Interface	Parameters (defaults)
`rankfilter_dpc3_p1`	AXI4-Stream	`W` (8), `AW` (11), `USE_MAP` (1)
`rankfilter_dpc3_p1_v`	video timing	`W` (8), `AW` (11), `USE_MAP` (1)

1 pixel per clock. `AW` = 11 holds 2,048-pixel lines; `USE_MAP` = 0 removes the flag. The ASIC set has the same cores with an `_asic` suffix; SEU-tolerant variants (`_seu`) are in DS-RF-04.

Deliverables

- Verilog-2005 source, FPGA and ASIC sets
- The integration packages listed above
- Reference model, vectors with an example map
- Self-checking SystemVerilog testbench
- Coverage report, Lean 4 proof files, integration notes

Licensing: source code, per project or per company; pricing and terms on request. Simulation evaluation package on request.

Bumble Bytes Ltd · registered in England and Wales, company number 16457148 · contact@bumblebytes.co.uk · bumblebytes.co.uk/fpga

Revision 1.0, 2026-10-14, first release. Specifications may change without notice. The information is provided as is, with no warranty beyond the terms of the licence agreement. AMD, Artix, UltraScale+, Vivado and Zynq are trademarks of Advanced Micro Devices, Inc.; Altera, Cyclone and Quartus of Altera Corporation; Lattice and ECP5 of Lattice Semiconductor Corporation; Arm, AMBA and AXI of Arm Limited. Other names are the property of their owners.