RANKFILTER IP CORE DATASHEET

Bayer defect-pixel correction

Hot and dead pixel correction, or a same-colour 3×3 median, on raw Bayer sensor data

Datasheet DS-RF-02 · Revision 1.0 · 2026-10-14 · Bumble Bytes Ltd

Description

The RankFilter Bayer cores correct hot and dead pixels in a raw Bayer stream, before demosaicing, at 1, 2 or 4 pixels per clock. Each raw pixel is compared with the median of the nine same-colour pixels around it and replaced only when it differs by more than a run-time threshold. With correction off, the core is a same-colour median filter.

The median comes from a comparator network, a fixed sequence of compare-and-swap steps that maps directly into logic. It sorts each same-colour column once and shares the result between neighbouring windows. This column-sharing method needs 13 comparators per raw pixel, against 19 for a network that sorts each window on its own. The complete 1 pixel per clock core uses 410 LUTs and 2 RAMB36 on Artix 7, 15 % fewer LUTs than the same core built with the 19-comparator network.

The median network is proved correct in the Lean 4 proof assistant, and the flow control is formally proved with SymbiYosys. Each core is one Verilog-2005 file with its line buffer and border logic, using only inferred block RAM, so it suits any FPGA or ASIC flow.

Applications

- Hot and dead pixel correction in colour cameras for machine vision, industrial, scientific and broadcast use
- Same-colour impulse-noise filtering on raw sensor data

FUNCTION

- Median of the 9 same-colour pixels at offsets −2, 0 and +2 (a 5×5 raw neighbourhood)
- Correction: replace a pixel only if it differs from that median by more than `cfg_dpc_thr`
- Any 2×2 colour pattern: RGGB, GRBG and others
- Same-colour edge replication or a constant at the borders

INTERFACES

- AXI4-Stream video with full back-pressure (TUSER frame start, TLAST line end)
- Video-timing variant at 1 px/clk for sources that cannot stall
- One clock; synchronous reset (`aresetn` in the Vivado package)

PERFORMANCE AND SIZE

- 1, 2 or 4 raw pixels per clock (px/clk)
- 4K60 raw at 4 px/clk and 148.5 MHz on Artix 7, Zynq and Cyclone V, with the line buffer set to 4,096 pixels (one parameter)
- Longest line 2,048 pixels by default (4,096 at 2 px/clk), parameter `AW`
- 13 comparators per raw pixel (11.5 at 4 px/clk); latency 2 lines + 29 clocks
- Pixel width set by a parameter; tested at 8 to 16 bits

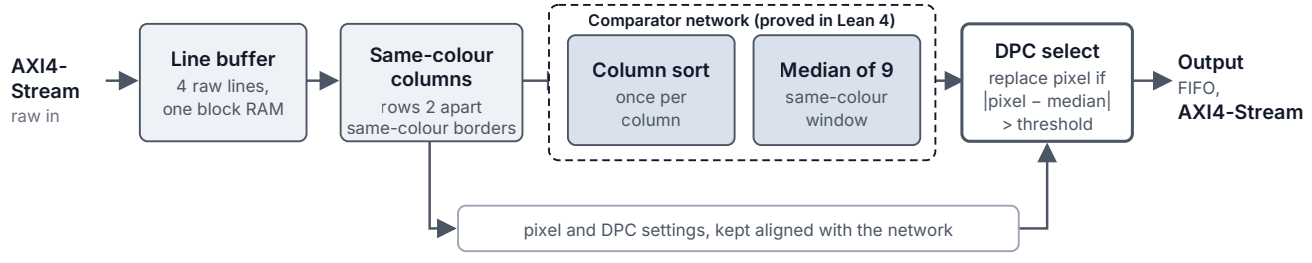
VERIFICATION

- Median network proved correct in Lean 4
- Flow control formally proved (SymbiYosys)
- Self-tested on Cyclone V silicon

INTEGRATION

- One Verilog-2005 file per core, for any FPGA or ASIC flow
- Vivado 2025.2 IP Integrator, Quartus Platform Designer and VHDL packages; ASIC set

Block diagram



At 2 and 4 px/clk two colour cores run side by side. The video-timing core has no output FIFO.

The DPC select stage takes two clocks: subtract, then compare and select. Border pixels are generated inside the core.

Implementation results

Device and resource	1 px/clk	2 px/clk[1]	4 px/clk	Video timing, 1 px/clk
AMD Artix 7 xc7a35t-1 · Vivado 2025.2				
LUTs	410	649	1,197	282
Flip-flops	771	1,116	1,860	635
Block RAM (RAMB36)	2	4	2	2
Fmax (MHz)	228	213	215	233
AMD Zynq UltraScale+ xczu3eg-1 · Vivado 2025.2				
LUTs	415	639	1,136	284
Fmax (MHz)[2]	571	571	575	571
Altera Cyclone V 5CEBA4F23C8 · Quartus Prime Lite 19.1				
ALMs	435	683	1,115	342
Block RAM (M10K)	9	17	11	7
Fmax (MHz), lowest of 3 seeds[3]	159	180	180	180
Lattice ECP5 LFE5U-85F −6 · yosys and nextpnr				
LUT4s	1,092	1,701	2,673	681
Flip-flops	1,019	1,469	2,458	922
Block RAM (DP16KD)	4	8	15	4
Fmax (MHz), lowest of 5 seeds[4]	159	152	150	163

Figures are for the complete core with correction on and 8-bit pixels, at the slowest speed grade, with line buffers for 2,048-pixel lines. [1] The 2 px/clk core at its shipped default of 4,096-pixel lines. AMD: post-route, filter alone, resources at 148.5 MHz, Fmax from a separate sign-off run per design. Cyclone V and ECP5 include a small test harness. [2] Block RAM clock limit of the −1 part. [3] Video timing: 2 seeds; Cyclone V C8 limits M10K to 180 MHz. [4] Video timing: 3 seeds. Wider pixels and Zynq 7000: product guide PG-RF-02 (available on request).

Comparison

Against the same core built with the 19-comparator single-window network (same wrapper, correction stage and flow), RankFilter uses 15 % fewer LUTs on Artix 7 (410 against 485), 16 % fewer on Zynq UltraScale+, 10 % fewer ALMs on Cyclone V and 15 % fewer LUT4s on ECP5. In a 3×3 filter the comparator network is about a quarter of the logic; synthesised on its own it is 39 % smaller (ECP5).

Verification

Lean 4 proves that the 3×3 median networks, including the two-lane networks used at 4 px/clk, output the median for any ordered pixel type, and SymbiYosys proves the flow control of the 1, 2 and 4 px/clk cores for any handshake pattern. Each complete filter matches a bit-exact reference model with full-rate, stalled and random back-pressure, random thresholds, 1080p and 4K frames and 8 to 16-bit pixels. In 73,577 malformed-input runs across all 24 RankFilter cores (truncated frames, missing or extra TUSER), no core hung, and each returned to correct output by itself. On Cyclone V silicon the 1 px/clk core, with correction on, filtered the same two test frames under random back-pressure about 3 million times with no CRC-32 mismatch.

Core family

Module	Raw px/clk	Interface
`rankfilter_bayer3_p1`	1	AXI4-Stream
`rankfilter_bayer3_p2`	2	AXI4-Stream
`rankfilter_bayer3_p4`	4	AXI4-Stream
`rankfilter_bayer3_p1_v`	1	video timing

The ASIC set has the same cores with an `_asic` suffix. The Bayer cores correct by threshold; the monochrome cores (DS-RF-03) also take a static defect map.

Deliverables

- Verilog-2005 source, FPGA and ASIC sets
- The integration packages listed above
- Bit-exact Python reference model, golden vectors
- Self-checking SystemVerilog testbench
- Board self-test with an expected CRC-32
- Lean 4 proof files and integration notes

Licensing: source code, per project or per company; pricing and terms on request. Simulation evaluation package on request.

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