RANKFILTER IP CORE DATASHEET

Median and rank filters

3×3, 5×5 and 7×7 median and percentile filters for FPGA and ASIC video

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Description

The RankFilter median and rank filters replace each pixel of a video stream with the median, or a chosen percentile, of its 3×3, 5×5 or 7×7 neighbourhood: the k-th smallest of the window's values (k = 13 of 25 for a 5×5 median). A median removes impulse noise and isolated bad pixels and keeps edges sharp; a low or high percentile works as a grey-scale erosion or dilation.

Each core is built from comparator networks, fixed sequences of compare-and-swap steps that map directly into logic, and shares them between neighbouring windows. Each column is sorted once and reused by every window that contains it, and the networks that merge the sorted columns come from a computer search. A 5×5 median needs 52 comparators per output pixel, against 63 for column sharing (Adams 2021), the lowest published count we know of. In the same Vivado flow the complete 5×5 filter uses 871 LUTs on Artix 7, a quarter of the LUTs of AMD's Vitis Vision `medianBlur`.

The comparator networks are proved correct in the Lean 4 proof assistant for any pixel width, and the flow control is formally proved with SymbiYosys. Each core is one Verilog-2005 file with its line buffers and border logic, using only inferred block RAM, so it suits any FPGA or ASIC flow. At 4 pixels per clock a core filters 4K60 video from a 148.5 MHz clock.

Applications

- Impulse (salt-and-pepper) noise removal in camera and broadcast video
- Pre-processing for machine vision and inspection
- Grey-scale erosion and dilation with the 25th and 75th percentiles
- Rank filtering in medical and scientific imaging

FUNCTION

- 3×3, 5×5 and 7×7 median; 5×5 25th and 75th percentile
- One output pixel per input pixel, in raster order
- Replicate or constant borders, set at run time

INTERFACES

- AXI4-Stream video with full back-pressure (TUSER frame start, TLAST line end)
- Video-timing variants for sources that cannot stall
- One clock; synchronous reset (`aresetn` in the Vivado package)

PERFORMANCE AND SIZE

- 1, 2 or 4 pixels per clock (px/clk)
- 4K60 at 4 px/clk and 148.5 MHz on Artix 7, Zynq and Cyclone V, with the line buffer set to 4,096 pixels (one parameter)
- Longest line 2,048 pixels by default (parameter `AW`)
- 5×5 on Artix 7: 871 LUTs, 2 RAMB36; latency 2 lines + 38 clocks
- Pixel width set by a parameter; tested at 8 to 16 bits

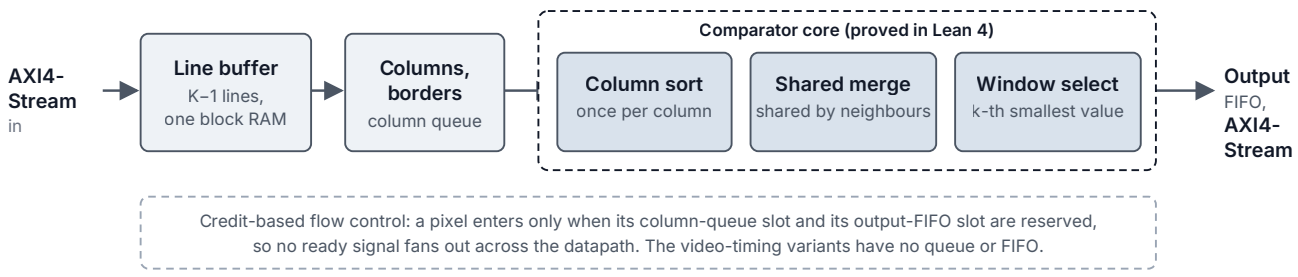
VERIFICATION

- Comparator networks proved correct in Lean 4
- Flow control formally proved (SymbiYosys)
- Self-tested on Cyclone V silicon

INTEGRATION

- One Verilog-2005 file per core, for any FPGA or ASIC flow
- Vivado 2025.2 IP Integrator, Quartus Platform Designer and VHDL packages; ASIC set

Block diagram



The 3×3 core at 1 px/clk has no shared merge stage. Border pixels are generated inside the core.

Implementation results

Device and resource	3×3, 1 px/clk	5×5, 1 px/clk	7×7, 1 px/clk	5×5, 4 px/clk	7×7, 4 px/clk
AMD Artix 7 xc7a35t-1 · Vivado 2025.2					
LUTs	345	871	1,969	2,638	5,534
Flip-flops	567	1,511	3,458	3,766	7,976
Block RAM (RAMB36)	1	2	3	2	3
Fmax (MHz)	237	209	217	225	215
AMD Zynq UltraScale+ xczu3eg-1 · Vivado 2025.2					
LUTs	344	957	2,052	2,797	6,023
Fmax (MHz)[1]	571	571	571	565	568
Altera Cyclone V 5CEBA4F23C8 · Quartus Prime Lite 19.1					
ALMs	371	896	1,941	2,216	5,276
Block RAM (M10K)	7	10	20	28	46
Fmax (MHz), lowest of 3 seeds[2]	180	180	167	163	152
Lattice ECP5 LFE5U-85F −6 · yosys and nextpnr					
LUT4s	928	2,056	4,455	5,184	11,452
Flip-flops	691	1,905	4,612	6,600	14,490
Block RAM (DP16KD)	2	4	6	15	23
Fmax (MHz), lowest of 5 seeds	146	162	150	154	128

Figures are for the complete filter with 8-bit pixels and 2,048-pixel line buffers, at the slowest speed grade. AMD: post-route, filter alone, resources at 148.5 MHz, Fmax from a separate sign-off run per design. Cyclone V and ECP5 include a small test harness. [1] Block RAM clock limit of the −1 part. [2] Cyclone V C8 limits M10K to 180 MHz. All 16 cores, Zynq 7000, 4K line buffers, wider pixels, power and ASIC: product guide PG-RF-01 (available on request).

Comparison

Against AMD Vitis Vision `medianBlur` in the same Vivado flow (Artix 7, 148.5 MHz, same line length): 59, 75 and 83 % fewer LUTs at 3×3, 5×5 and 7×7 (1 px/clk) and less block RAM in all configurations (comparison brief CB-RF-01). Against baselines built with the same generator and flow (column sharing; a pruned sorter for the 25th percentile; the 19-comparator single-window network at 3×3): 14 to 26 % fewer LUTs on Artix 7, 11 to 24 % on Cyclone V and ECP5.

Verification

Lean 4 proves that each comparator network outputs the k-th smallest value for any ordered pixel type. The generated RTL is simulated on all windows of 0s and 1s (all 2^{25} at 5×5; at 7×7 the column sorter on all 128 columns and the core on all combinations of sorted columns); a comparator network that is correct for all inputs of 0s and 1s is correct for all inputs (the 0-1 principle). Each complete filter matches a bit-exact reference model on random, 1080p and 4K frames at 8 to 16 bits. In 73,577 malformed-input runs across all 24 RankFilter cores (truncated frames, missing or extra TUSER), no core hung, and each returned to correct output by itself. On Cyclone V silicon, four of these cores filtered the same two test frames under random back-pressure about 19 million times with no CRC-32 mismatch.

Core family

Filter	AXI4-Stream	Video timing
3×3 median	1, 2, 4 px/clk	1 px/clk
5×5 median	1, 2, 4 px/clk	1 px/clk
5×5 25th percentile	1 px/clk	1 px/clk
5×5 75th percentile	1 px/clk	1 px/clk
7×7 median	1, 2, 4 px/clk	1 px/clk

16 cores, such as `rankfilter_k5_r13_p4`: 5×5, rank 13 (13th smallest), 4 px/clk. `_v`: video timing; `_asic`: ASIC set.

Deliverables

- Verilog-2005 source, FPGA and ASIC sets
- The integration packages listed above
- Bit-exact Python reference model, golden vectors
- Self-checking SystemVerilog testbench
- Board self-test with an expected CRC-32
- Lean 4 proof files and integration notes

Licensing: source code, per project or per company; pricing and terms on request. Simulation evaluation package on request.

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