RANKFILTER COMPARISON BRIEF

# RankFilter versus AMD Vitis Vision `medianBlur`

AMD's Vitis Vision Library includes a free median filter, `xf::cv::medianBlur`. We built it with Vitis HLS and implemented both designs in the same Vivado flow, harness and parts.

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**−75 %**
LUTs at 5×5, 1 px/clk: 871 against 3,490 on Artix 7 at 148.5 MHz

**−83 %**
LUTs at 7×7, 1 px/clk: 1,969 against 11,712; −82 % estimated power

**Does not fit**
Vitis 7×7 at 4 px/clk on an Artix 7 35T, where RankFilter uses 27 %. On a ZU3EG Vitis takes 63 % of the LUTs, RankFilter 9 %

**Less BRAM**
in all configurations, at 2,048- and 4,096-pixel lines (0.5 to 1.5 RAMB36 fewer)

## Measured on AMD Artix 7 xc7a35t-1 at 148.5 MHz (Vivado 2025.2, post-route)

| Window, px/clk | Vitis LUT | FF | RAMB36 | Power, mW[1] | RankFilter LUT | FF | RAMB36 | Power, mW[1] | Change: LUT, FF, power |
|---|---|---|---|---|---|---|---|---|---|
| 3×3, 1 | 846 | 1,280 | 1.5 | 29 | 345 | 567 | 1 | 15 | −59, −56, −48 % |
| 3×3, 2 | 1,089 | 2,027 | 1.5 | 39 | 551 | 867 | 1 | 26 | −49, −57, −33 % |
| 3×3, 4 | 1,710 | 3,398 | 1.5 | 63 | 974 | 1,526 | 1 | 48 | −43, −55, −24 % |
| 5×5, 1 | 3,490 | 4,911 | 2.5 | 123 | 871 | 1,511 | 2 | 45 | −75, −69, −63 % |
| 5×5, 2 | 4,043 | 8,898 | 2.5 | 184 | 1,333 | 2,069 | 2 | 63 | −67, −77, −66 % |
| 5×5, 4 | 7,346 | 16,912 | 2.5 | 260 | 2,638 | 3,766 | 2 | 121 | −64, −78, −53 % |
| 7×7, 1 | 11,712 | 15,988 | 3.5 | 618 | 1,969 | 3,458 | 3 | 109 | −83, −78, −82 % |
| 7×7, 4 | Does not fit: needs about 24,000 LUTs (24,016 in the Zynq 7000 build); the device has 20,800 | | | | 5,534 | 7,976 | 3 | 292 | Fits |

Vivado 2025.2, default directives, filter instance only (the measurement harness is excluded), 8-bit pixels, 2,048-pixel lines on both sides. Resources and power at a common 148.5 MHz constraint; repeating each implementation at 6.60 and 6.90 ns changed LUT and FF counts by at most 0.2 %. Vitis: Vitis_Libraries 2025.2 (tag v2025.2_update2) as shipped, built with Vitis HLS 2025.2 at two clock targets, 148.5 MHz and 250 MHz. The two builds trade LUTs against flip-flops, so each Vitis figure is the better of the two: the reading most favourable to Vitis. [1] Power is Vivado's vectorless estimate, not a measurement. The 7×7 at 2 px/clk is not compared (see the method below).

### Other AMD parts at 148.5 MHz

| Part | RankFilter LUTs against Vitis | Flip-flops | Vitis 7×7 at 4 px/clk |
|---|---|---|---|
| Zynq 7000 xc7z020-1 | −45 to −83 % | −54 to −87 % | Fits: 24,016 LUTs, 45 % of the device, against RankFilter's 5,533 (−77 %) |
| Zynq UltraScale+ MPSoC xczu3eg-1 | −58 to −86 % | −4 to −62 % | Fits: 44,460 LUTs, 63 % of the device, against RankFilter's 6,023 (−86 %) |

Same configurations, method and line length as the Artix 7 table. The fast HLS target is 250 MHz on Zynq 7000 and 333 MHz on Zynq UltraScale+. On UltraScale+ the Vitis builds use few flip-flops, so RankFilter saves only 4 % of flip-flops at 3×3, 4 px/clk.

## Where Vitis is level or ahead

| | |
|---|---|
| Speed | Both sign off at about the same Fmax on 7-series parts: Vitis 202 to 220 MHz, RankFilter 209 to 237 MHz on Artix 7. Speed is not a reason to switch |
| Close cases | Estimated power at 3×3, 4 px/clk on Zynq 7000 (RankFilter +2 %). Flip-flops on Zynq UltraScale+, where RankFilter saves only 4 % at 3×3, 4 px/clk. Elsewhere RankFilter is smaller on each metric |
| Price and support | `medianBlur` is free and supported by AMD inside the Vitis flow. RankFilter is licensed |

## What else RankFilter offers

| | |
|---|---|
| Portability | Verilog-2005 for AMD, Altera and Lattice FPGAs, plus an ASIC set; Vivado, Quartus and VHDL packages |
| Proofs | Comparator networks proved in Lean 4; flow control formally proved (SymbiYosys) |
| Silicon | Five cores ran a soak test on Cyclone V: about 22 million runs, zero CRC-32 mismatches |
| Beyond the median | Percentiles; Bayer and monochrome defect-pixel correction; SEU-tolerant and video-timing variants |
| Other designs | 14 to 26 % fewer LUTs on Artix 7 than baselines built with the same generator and flow (column sharing; a pruned sorter for the 25th percentile; the 19-comparator single-window network at 3×3) |

## With 4,096-pixel (4K) lines, Artix 7 at 148.5 MHz

| Window, px/clk | Vitis LUT | FF | RAMB36 | RankFilter LUT | FF | RAMB36 | Change: LUT, FF |
|---|---|---|---|---|---|---|---|
| 3×3, 1 | 863 | 1,309 | 3 | 346 | 573 | 2 | −60, −56 % |
| 3×3, 2 | 1,078 | 2,058 | 3 | 544 | 872 | 2 | −50, −58 % |
| 3×3, 4 | 1,748 | 3,429 | 3 | 970 | 1,531 | 2 | −45, −55 % |
| 5×5, 1 | 3,523 | 4,917 | 5 | 871 | 1,518 | 4 | −75, −69 % |
| 5×5, 2 | 4,043 | 8,953 | 5 | 1,321 | 2,075 | 4 | −67, −77 % |
| 5×5, 4 | 7,364 | 16,943 | 5 | 2,636 | 3,772 | 4 | −64, −78 % |
| 7×7, 1 | 11,767 | 16,029 | 7 | 1,969 | 3,465 | 5.5 | −83, −78 % |
| 7×7, 4 | Does not fit the xc7a35t | | | 5,526 | 7,983 | 5.5 | Fits |

Same flow, constraint and method as the 2,048-pixel table; Vitis built with `MAX_COLS` = 4096, RankFilter with the line buffer set to 4,096 pixels. These Vitis builds use the same source as the co-simulated 2,048-pixel builds and were not co-simulated themselves. The 7×7 at 2 px/clk is not compared.

## Why the gap

`medianBlur` sorts all $K^2$ pixels of every window with an odd-even transposition network and starts each window from scratch: 36, 300 and 1,176 compare-exchanges per pixel at 3×3, 5×5 and 7×7, before synthesis removes unused ones. RankFilter sorts each column once and shares the work between neighbouring windows: 52 per pixel at 5×5, 1 px/clk, and 37 at 2 or 4 px/clk.

## Method and limits of the comparison

Both designs went through the same harness, Vivado version, directives, parts, line length and 148.5 MHz constraint. Fmax figures come from a separate sign-off run per design. At 4,096-pixel lines the result is the same (table above): LUTs −45 to −83 % on Artix 7 and less block RAM in all configurations.

HLS adds AXI4-Stream register slices and dataflow FIFOs. They stay in the Vitis figures, because a Vitis user gets them. Vitis has replicate borders only, where RankFilter also has a constant border, and it needs TLAST on every line.

Every Vitis build in this comparison was simulated as RTL against our reference model on 320×240 frames and gives the correct median; three representative builds (3×3 and 7×7 at 1 px/clk, 5×5 at 4 px/clk) were also simulated as synthesised netlists. The 7×7 configuration at 2 px/clk is excluded, because its output did not match the reference in our test.

The full method and raw data are in the Vivado sign-off report, available on request. Datasheets DS-RF-01 to DS-RF-04 summarise each product family; product guides PG-RF-01 to PG-RF-04 (available on request) give the RankFilter figures for each core and FPGA family.

## Revision history

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 2026-10-14 | First release |

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