FPGA sign-off sprint

Independent evidence for one FPGA block, at a fixed price: implementation results on AMD, Altera and Lattice parts, a like-for-like comparison with the vendor's free core, verification to coverage closure, formal interface checks and upset testing. You get a report and every script needed to run it again.

We built this flow for our own RankFilter cores, and it produced the figures in their datasheets. The same scripts can be pointed at your block. Typical buyers are IP vendors before a release, teams deciding between their own core and a free vendor core, and space teams who need upset evidence before a beam test.

Packages

Sign-off report

£2,400 fixed

about 1 week

- Implementation in Vivado, Quartus and the open Lattice ECP5 flow, on up to 3 parts you choose
- LUT, flip-flop, block RAM and Fmax per part, over several placement seeds
- Comparison with the vendor's free core, or your own baseline, in the same harness, flow and clock constraint

Verification sprint

£5,900 fixed

about 3 weeks

- Everything in the sign-off report
- Verilator testbench checked against your reference model, or a Python model we write
- Coverage to closure, with every remaining gap explained
- SymbiYosys properties on AXI4-Stream or AXI4-Lite handshakes
- Malformed-input runs: lost and doubled beats, short frames, size changes

Upset campaign

£2,900 fixed

add-on, about 1 week

- Single-event upsets injected in simulation into flip-flops and block RAM
- Each run classed: no effect, recovers alone, needs a reset; with 95 % intervals
- Recovery time per upset and the state bits that cause hangs
- Suggested checks for those bits, with their LUT cost

Prices are for one block of up to about 10,000 LUTs with a written interface description. Larger blocks and follow-on work are quoted, or charged at £450 a day.

What you receive

- A short report: results tables, method, and what the evidence does not cover
- The testbench, properties, constraints and run scripts, yours to keep and rerun in CI
- Logs and reports from each tool, so every number traces back to a run

How it works

- All work is done remotely. Your source stays on our machines under NDA and is deleted at hand-over if you ask
- Vivado 2025.2 ML Standard and Quartus Prime Lite device support; larger parts by arrangement
- Half the fee at the start, half on delivery
- £2m professional indemnity insurance (PolicyBee)

Example: the same work on RankFilter

Against a free vendor core	AMD Vitis Vision *medianBlur* and RankFilter built in the same Vivado flow at 148.5 MHz: 75 % fewer LUTs at 5×5 and 83 % at 7×7. The report also shows where the vendor core is level, and the one Vitis build that gave wrong output (excluded). Comparison brief CB-RF-01.
Multi-vendor sign-off	24 cores on Artix 7, Zynq 7000 and Zynq UltraScale+ (Vivado), Cyclone V (Quartus) and ECP5 (nextpnr), plus sky130 and ASAP7 ASIC trials.
Upsets	8,000 random flip-flop upsets per core. The default core needed a reset in 4.7 % of runs (95 % interval 4.2 to 5.2 %); the hardened core, with 72 extra LUTs of checks, needed none. Datasheet DS-RF-04.
Verification	100 % block and expression coverage; flow control proved in SymbiYosys; 73,577 malformed-input runs across 24 cores, with no hang and correct output restored each time; about 22 million self-test runs on Cyclone V hardware with no errors.

Datasheets, the comparison brief and a demo video: https://bumblebytes.co.uk/fpga/

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